

What is claimed is:

- 1 1. An logic unit comprising:
  - 2 a first logic unit connected to a first supply voltage;
  - 3 a second logic unit connected to a second supply voltage; and
  - 4 a voltage-level converter connecting the first logic unit to the second logic unit,
  - 5 the voltage-level converter including at least one transistor having a threshold voltage
  - 6 greater than or about equal to the difference between the second supply voltage and the
  - 7 first supply voltage and the at least one transistor connected to the second supply voltage.
- 1 2. The logic unit of claim 1, wherein the first logic unit comprises a memory unit.
- 1 3. The logic unit of claim 2, wherein the second logic unit comprises an arithmetic unit.
- 1 4. The logic unit of claim 3, wherein the one transistor comprises an insulated-gate field-effect transistor.
- 1 5. The logic unit of claim 4, wherein the insulated-gate field-effect transistor  
2 comprises a *p-type* insulated-gate field-effect transistor.
- 1 6. The logic unit of claim 1, wherein the voltage-level converter comprises an inverter.
- 1 7. The logic unit of claim 6, wherein the inverter comprises an *n-type* insulated-gate field-effect transistor connected in series with the at least one transistor.
- 1 8. The logic unit of claim 6, wherein the second logic unit comprises a clock distribution circuit.

1       9.     The logic unit of claim 6, where the voltage-level converter comprises a first  
2 inverter coupled in series to a second inverter.

1       10.    The logic unit of claim 9, wherein the first inverter includes the at least one  
2 transistor.

1       11.    A logic unit comprising:  
2            a first logic unit connected to a first supply voltage;  
3            a second logic unit connected to a second supply voltage; and  
4            a logic circuit connecting the first logic unit to the second logic unit, the logic  
5 circuit including at least one transistor having a threshold voltage greater than or about  
6 equal to the difference between the second supply voltage and the first supply voltage  
7 and the at least one transistor connected to the second supply voltage .

1       12.    The logic unit of claim 11, wherein the logic circuit comprises an AND circuit.

1       13.    The logic unit of claim 11, wherein the logic circuit comprises a NAND circuit.

1       14.    The logic unit of claim 11, wherein the logic circuit comprises an OR circuit.

1       15.    The logic unit of claim 11, wherein the logic circuit comprises a NOR circuit.

1       16.    The logic unit of claim 11, wherein the logic circuit comprises an XOR circuit.

1       17.    The logic unit of claim 11, wherein the second logic unit comprises a clock  
2 distribution circuit.

1       18.    The logic unit of claim 17, wherein the logic circuit comprises a NAND circuit.

1       19.    The logic unit of claim 17, wherein the logic circuit comprises a NOR circuit.

1       20.     The logic unit of claim 11, wherein the second logic unit comprises an arithmetic  
2       unit.

1       21.     The logic unit of claim 20, wherein the logic circuit comprises an OR circuit.

1       22.     The logic unit of claim 20, wherein the logic circuit comprises an XOR circuit.

1       23.     A method comprising:

2              transmitting a logic signal from a logic unit having an output voltage swing  
3       between a first voltage level and a second voltage level, the first voltage being greater  
4       than the second voltage level;

5              receiving the logic signal at a logic circuit having a pull-up transistor and an  
6       output voltage swing between a third voltage level and a fourth voltage level, the third  
7       voltage being greater than the fourth voltage level; and

8              turning off the pull-up transistor when the logic signal has a value slightly greater  
9       than the difference between the third voltage level and the first voltage level, the third  
10      voltage level being greater than the first voltage level.

1       24.     The method of claim 23, further comprising:

2              generating an output logic signal at the logic circuit, the output logic signal having  
3       a voltage swing between the third voltage level and the fourth voltage level; and

4              receiving the output logic signal at an inverter having an output voltage swing  
5       between the third voltage level and the fourth voltage level.

1       25.     The method of claim 23, further comprising:

2              generating an output logic signal at the logic circuit, the output logic signal having  
3       a voltage swing between the third voltage level and the fourth voltage level; and

4              receiving the output logic signal at a logic circuit having an output voltage swing  
5       between the third voltage level and the fourth voltage level.